Assignee: Intel Compration

REMARKS

Applicant respectfully requests reconsideration of this application as amended. Claims 1, 3 through 5, 7 through 15, and 17 through 21 are pending in this application. Claims 2, 6, 16, and 22 were previously cancelled. Claims 19 through 22 were previously added.

SECTION 103 ISSUES

In the Final Office Action, at paragraph 3, claims 1, 3 through 5, 7 through 11, 15, and 17 through 21 stand rejected under 35 U.S.C. §103(a) as being anticipated by Huang, et al., U.S. patent number 6,131,134 (hereinafter *Huang*), in view of Rafferty et al., U.S. patent number 6,141,719 (hereinafter *Rafferty*) and Pollard, et al., U.S. patent number 5,754,870 (hereinafter *Pollard*). Applicant respectfully traverses.

In the Final Office Action at paragraph 3, in reference to claim 1, it was admitted that "Huang, as modified by Rafferty, does not teach influencing said detach control signal with a wake-up signal sent on a wake-up signal wire separate from said data transmission wires of said data bus from said near end of said data bus to said far end of said data bus." The Office Action then claims that *Pollard* discloses these claim limitations. Applicant wishes to point out that *Pollard* presents a set of mating *connectors* 26, 28 and does not expressly teach *any* data bus between the host computer 22 and the plug-in card 30. At the most some sort of *parallel* data bus may be *inferred* due to the characterization

Assignee: Intel Commation

of connectors 26, 28 as "preferably a standard 68-pin connector" (*Pollard* column 4 lines 17 through 22).

In order to more distinctly and clearly claim the present invention, applicant has amended independent claim 1 to now recite in pertinent part "a *serial* data bus." (Applicant's emphasis added.) This recitation in the method of claim 1 is supported in the specification on page 1, line 18 through page 2 line 2, identifying both the Universal Serial Bus data bus of Figures 1 through 6 and the IEEE-1394 data bus of Figures 7 through 9 as serial data busses. As the Final Office Action has admitted that the limitations cited above are not found in *Huang* or *Rafferty*, and as there is no support for such a limitation with respect to a *serial* data bus disclosed in *Pollard*, applicant therefore believes that amended independent claim 1 is allowable over the cited *Huang*, *Rafferty*, and *Pollard* references.

Because claims 3 through 5, and 7, depend from independent claim 1, and because applicant believes that independent claim 1 is now allowable, applicant further believes that claims 3 through 5, and 7, are now allowable.

In the Final Office Action at paragraph 3, in reference to claim 8, it was admitted that "Huang, as modified by Rafferty, does not teach a wake-up signal wire separate from said data transmission wires of said data bus to send a wake-up signal from said near end of said data bus to said far end of said data bus to influence said detach control signal."

The Office Action then claims that *Pollard* discloses these claim limitations. Applicant again wishes to point out that *Pollard* presents a

Assignee: Intel Compration

set of mating *connectors* 26, 28 and does not expressly teach *any* data bus between the host computer 22 and the plug-in card 30. At the most some sort of *parallel* data bus may be *inferred* due to the characterization of connectors 26, 28 as "preferably a standard 68-pin connector" (*Pollard* column 4 lines 17 through 22).

In order to more distinctly and clearly claim the present invention, applicant has amended independent claim 8 to now recite in pertinent part "a *serial* data bus." (Applicant's emphasis added.) This recitation in the apparatus of claim 8 is supported in the specification on page 1, line 18 through page 2 line 2, identifying both the Universal Serial Bus data bus of Figures 1 through 6 and the IEEE-1394 data bus of Figures 7 through 9 as serial data busses. As the Final Office Action has admitted that the limitations cited above are not found in *Huang* or *Rafferty*, and as there is no support for such a limitation with respect to a *serial* data bus disclosed in *Pollard*, applicant therefore believes that amended independent claim 8 is allowable over the cited *Huang*, *Rafferty*, and *Pollard* references.

Because claims 9 through 15, and 17, depend from independent claim 8, and because applicant believes that independent claim 8 is now allowable, applicant further believes that claims 9 through 15, and 17, are now allowable.

In the Office Action at paragraph 3, in reference to claim 15, it was admitted that "Huang, as modified by Rafferty, does not teach means for influencing said detach control signal with a wake-up signal sent on a wake-up signal wire separate from said data transmission wires of said

Assignee: Intel Compration

data bus from said near end of said data bus to said far end of said data bus." The Office Action then claims that *Pollard* discloses these claim limitations. Applicant again wishes to point out that *Pollard* presents a set of mating *connectors* 26, 28 and does not expressly teach *any* data bus between the host computer 22 and the plug-in card 30. At the most some sort of *parallel* data bus may be *inferred* due to the characterization of connectors 26, 28 as "preferably a standard 68-pin connector" (*Pollard* column 4 lines 17 through 22).

In order to more distinctly and clearly claim the present invention, applicant has amended independent claim 15 to now recite in pertinent part "a *serial* data bus." (Applicant's emphasis added.) This recitation in the apparatus of claim 15 is supported in the specification on page 1, line 18 through page 2 line 2, identifying both the Universal Serial Bus data bus of Figures 1 through 6 and the IEEE-1394 data bus of Figures 7 through 9 as serial data busses. As the Final Office Action has admitted that the limitations cited above are not found in *Huang* or *Rafferty*, and as there is no support for such a limitation with respect to a *serial* data bus disclosed in *Pollard*, applicant therefore believes that amended independent claim 15 is allowable over the cited *Huang*, *Rafferty*, and *Pollard* references.

Because claims 16 through 21 depend from independent claim 15, and because applicant believes that independent claim 15 is now allowable, applicant further believes that claims 16 through 21 are now allowable.

Assignee: Intel Corporation

In the Final Office Action at paragraph 3, in reference to claim 19, it was admitted that "Huang, as modified by Rafferty, does not teach a wake-up control signal separate from said data transmission wires of said data bus to send a wake-up signal from said near end of said data bus to said far end of said data bus; and said second circuit to send said detach control signal responsive to said wake-up signal." The Final Office Action then claims that *Pollard* discloses these claim limitations. Applicant again wishes to point out that *Pollard* presents a set of mating *connectors* 26, 28 and does not expressly teach *any* data bus between the host computer 22 and the plug-in card 30. At the most some sort of *parallel* data bus may be *inferred* due to the characterization of connectors 26, 28 as "preferably a standard 68-pin connector" (*Pollard* column 4 lines 17 through 22).

In order to more distinctly and clearly claim the present invention, applicant has amended independent claim 19 to now recite in pertinent part "a *serial* data bus." (Applicant's emphasis added.) This recitation in the system of claim 19 is supported in the specification on page 1, line 18 through page 2 line 2, identifying both the Universal Serial Bus data bus of Figures 1 through 6 and the IEEE-1394 data bus of Figures 7 through 9 as serial data busses. As the Final Office Action has admitted that the limitations cited above are not found in *Huang* or *Rafferty*, and as there is no support for such a limitation with respect to a *serial* data bus disclosed in *Pollard*, applicant therefore believes that amended independent claim 19 is allowable over the cited *Huang*, *Rafferty*, and *Pollard* references.

Assignee: Intel Comparation

Because claims 20 and 21 depend from independent claim 19, and because applicant believes that independent claim 19 is now allowable, applicant further believes that claims 20 and 21 are now allowable.

Assignee: Intel Corporation

SUMMARY

Applicant believes that all pending claims are allowable over the cited art of record. Applicant therefore respectfully requests that all pending claims 1, 3 through 5, 7 through 15, and 17 through 21 be allowed.

If the Examiner finds any remaining impediment to the prompt allowance of these claims that could be clarified with a telephone conference, the Examiner is respectfully requested to contact applicant's representative, Dennis A. Nicholls, at (408) 765-5789.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due.

Respectfully submitted,

Date: 12 Facamber, 2003

Dennis A. Nicholls Reg. No. 42,036 12400 Wilshire Blvd.

Seventh Floor

Los Angeles, CA 90025

(408) 765-5789

Attorney for Assignee Intel Corporation